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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/729,750	12/04/2003	Kenneth J. Goodnow	BUR9-2003-0100US1	3174

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EXAMINER	
TAT, BINH C	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 05/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/729,750	GOODNOW ET AL.	
	Examiner	Art Unit	
	Binh C. Tat	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/04/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/729750 filed on 12/04/03.

Claims 1-20 remain pending in the application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Kruse · James (U.S Patent 6530070).

3. As to claims 1, and 9 Kruse teaches a structure (fig 1c) and method (abstract), comprising: an FPGA (Field-programmable Gate Array) including a plurality of FPGA elements, each of the FPGA elements comprising an FPGA CLB (Configurable Logic Block) (see fig 1A-1C element 100, 110,120 and CLB array), wherein each FPGA element in the FPGA is assigned an address and is configured to provide its address (see fig 2c and 3a col 6 lines 2-67 and especially lines 34-42), wherein a first subset of the FPGA elements is configured to form a first functional block (see fig 1c, 2c, and fig 3a col 6 lines 2-67), wherein the first functional block comprises a mapped location register residing in one or more FPGA CLBS of the first functional block (see fig 1c, 2c, and fig 3a col 6 lines 2-67 especially lines 18-28), and wherein the mapped location register is configured to receive and store the address of a current location FPGA element (see fig 1c, 2c, and fig 3a col 6 lines 2-67 especially lines 18-28), the current location

FPGA element being in the first functional block and the address of the current location FPGA element being specified as the location of the first functional block (see fig 1c, 2c, 3a-3c, and 4 col 6 lines 17 to col 7 lines 58).

4. As to claims 2, and 10 Kruse teaches wherein the first functional block further comprises a mapped destination register residing in one or more FPGA CLBS of the first functional block, and wherein the mapped destination register is configured to receive and store the address of a destination FPGA element, the address of the destination FPGA element being specified as the destination of the first functional block (see fig 1c, 2c, and fig 3a col 6 lines 2-67 especially lines 18-28).

5. As to claims 3, and 11 Kruse teaches wherein the first functional block further comprises a mapped movement register residing in one or more FPGA CLBS of the first functional block, and wherein the mapped movement register is configured to receive and store the direction and distance of a next step of the movement of the first functional block (see fig 3a-3c and fig 4 col 6 lines 34 to col 7 lines 58).

6. As to claims 4, and 12 Kruse teaches wherein the first functional block further comprises a mapped logic location function configured to calculate the direction, distance, and time for the next step of the movement of the first functional block based on the contents of the mapped location register, the mapped destination register, and a time limit allowed for the movement of the first functional block (see fig 3a-3c and fig 4 col 6 lines 34 to col 7 lines 58).

7. As to claims 5, and 13 Kruse teaches further comprising a first localized I/0 (Input/output) circuit and a second localized I/0 circuit both electrically coupled to the FPGA, wherein the first functional block is formed via the first localized I/0 circuit, and wherein the first

functional block is configured to move to the second localized I/0 circuit (see fig 1c, 2c, and 3a-3d col. 2 lines 12-27 and col 6 line 17-57 and col 7 lines 1-29) .

8. As to claims 6, and 14 Kruse teaches wherein the first functional block is configured to move to the second localized I/0 circuit within a time limit in terms of clock cycles (see fig 1c, 2c, and 3a-3d, 4 col. 2 lines 12-27 and col 6 line 17-57 and col 7 lines 1-58).

9. As to claims 7, and 15 Kruse teaches wherein a second subset of the FPGA elements are configured to form a second functional block separate from the first functional block at any time, wherein the second functional block is formed via the first localized I/0 circuit, and wherein the second functional block is configured to move to the second localized I/0 circuit (see fig 1c, 2c, and 3a-3d, 4 col. 2 lines 12-27 and col 6 line 17-57 and col 7 lines 1-58).

10. As to claims 8, and 16 Kruse teaches wherein the FPGA further comprises connections electrically coupling each FPGA element to surrounding FPGA elements such that the contents of all FPGA elements in a functional block can be transferred to their non-adjacent FPGA elements in one clock cycle (see fig 1c, fig 3a-d col 6 line2-67).

11. As to claim 17 Kruse teaches a method for operating an FPGA, the method comprising the steps of: providing a plurality of FPGA elements, each of the plurality of FPGA elements comprising an FPGA CLB and being assigned an address (see fig 1A-1C, 2c and fig 3a element 100, 110,120 and CLB array and col. 6 lines 34-42); forming a first functional block comprising one or more FPGA elements of the plurality of FPGA elements (see fig 1c, 2c, and fig 3a col 6 lines 2-67 especially lines 18-28); moving the first functional block to a destination in the FPGA (see fig 2c, 3a-3d col 6 lines 2 to col 7 lines 26); and forming a second functional block comprising at least one FPGA element of the plurality of FPGA elements, the second functional

block being separate from the first functional block at any time (see fig 1c, 2c, 3a-3c, and 4 col 6 lines 17 to col 7 lines 58).

12. As to claim 18 Kruse teaches wherein the step of forming the first functional block comprises the step of assigning all the FPGA elements of the first functional block a unique function number (see fig 2c, 3a-3d col 6 lines 2 to col 7 lines 26, wherein the unique function number is 301 in fig 3a and 3b).

13. As to claim 19 Kruse teaches wherein the step of forming the first functional block comprises the steps of: forming a mapped location register residing in one or more FPGA CLBS of the first functional block (see fig 1c, 2c, and fig 3a col 6 lines 2-67 especially lines 18-28); forming a mapped destination register residing in one or more FPGA CLBS of the first functional block (see fig 1c, 2c, and fig 3a col 6 lines 2-67 especially lines 18-28); loading the mapped location register with the address of a current location FPGA element, the current location FPGA element being in the first functional block and the address of the current location FPGA element being specified as the location of the first functional block(see fig 2c, 3a-3d col 6 lines 2 to col 7 lines 26); and loading the mapped destination register with the address of a destination FPGA element, the address of the destination FPGA element being specified as the destination of the first functional block (see fig 1c, 2c, and fig 3a col 6 lines 2-67 especially lines 18-28).

14. As to claim 20 Kruse teaches the step of moving the first functional block to the destination in the FPGA comprises the steps of: forming a mapped logic location function in the first functional block (see fig 1c, 2c, and fig 3a col 6 lines 2-67 especially lines 18-28); and using the mapped logic location function to calculate the direction, distance, and time for the next step

of the movement of the first functional block based on the contents of the mapped location register, the mapped destination register, and the time limit allowed for the movement of the first functional block (see fig 3a-3c and fig 4 col 6 lines 34 to col 7 lines 58); and moving all the FPGA elements having the unique function number according to the calculated direction, distance, and time for the next step (see fig 2c, 3a-3d col 6 lines 2 to col 7 lines 26).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh C. Tat whose telephone number is (571) 272-1908. The examiner can normally be reached on 7:30 - 4:00 (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Binh Tat
Art unit 2825
April 15, 2005

A. M. Thompson
Primary Examiner
Technology Center 2800